

SPI'2009

**13th Workshop on
SIGNAL PROPAGATION ON INTERCONNECTS
May 12-15, 2009
Strasbourg, France**

Program

Tuesday May 12th

18:30-19:30 Workshop Registration

19:30 Welcome reception

Wednesday May 13th

8:15-9:00 Workshop Registration

9:00-9:10 Welcome & Opening Session

9:10-10:10 **Keynote**
**Importance of Signal Integrity Simulations in Early Design Phase of Product Design:
 From Component to System Level**
Ali Arslan (Nokia Corporation)

10:15-10:55 **Session 1: Packaging and Power Integrity**
 Session chair: Vittorio Ricchiuti, TechnoLabs R&D (I)

10:15-10:35 **Fast Analysis of Power Distribution Networks using Waveform Relaxation**
Ram Achar, Michel Nakhla, Arvind Sridhar, Harjot Dhindsa, Douglas Paul

10:35-10:55 **Characterization and modeling of the power delivery networks of memory chips**
I.S. Stievano, I.A. Maio, L. Rigazio, F.G. Canavero, R.Izzi, A.Girardi, T. Cunha, H. Teixeira, J.C. Pedro

11:00-11:30 Coffee Break

11:30-12:30 **Session 2: Transmission Lines and High-Speed Channels**
 Session chair: Roni Khazaka, Univ. McGill (CAN)

11:30-11:50 **Experimental Validation of the RC-Interconnect Effect Equalization with Negative Group Delay Active Circuit in Planar Hybrid Technology**
Blaise Ravelo, André Pérennec and Marc Le Roy

11:50-12:10 **Multi-Gigabit Serial Link Emissions and Mobile Terminal Antenna Interference**
Martti Voutilainen, Markku Rouvala, Pia Kotiranta, Tapani von Rauner

12:10-12:30 **Compromised Impedance Match Design for Signal Integrity of Pogo Pins Structures with Different Signal-Ground Patterns**
Ruey-Bo Sun, Ruey-Beei Wu, and Shih-Wei Haiso

12:30-14:00 Lunch

14:00-15:00 **Session 3: 3DModeling**
 Session chair: Flavio G. Canavero, Politecnico di Torino, Dipartimento di Elettronica, Torino (I)

14:00-14:20 **An Equivalent Circuit Model for the Identification of the Stub Resonance due to Differential Vias on PCB**
Vittorio Ricchiuti; Francesco de Paulis; Antonio Orlandi

14:20-14:40 **High Frequency Characterization and Modeling of High Density TSV in 3D Integrated Circuits**
C. Bermond, L. Cadix, A. Farcy, T. Lacrevez, B. Fléchet, P. Leduc

14:40-15:00 **Investigation of the Interactions Between Vias and the Power-Bus**
Gerd Heinrich, Stefan Dickmann

15:10-16:10 **Session 4: New interconnect technology**
 Session chair: Uwe Arz, Physikalisch-Technische Bundesanstalt, Braunschweig (D)

15:10-15:30 **Signal Integrity Analysis of Carbon Nanotube on-chip Interconnects**
A.G. Chiariello, A. Maffucci, G. Miano

15:30-15:50 **Self Consistent Simulation of Optoelectronic Circuits using a SPICE like Framework**
P. Gunupudi, T. Smy, J. Klein and J. Jakubczyk

15:50-16:10 **Signal Integrity of Femtosecond Pulses Patterns in a 500Gb/s All-Optical Demultiplexer for OTDM Interconnections by using Nonlinearities in Semiconductor Optical Amplifiers**
C. Crognale, and A. Di Giansante

16:10 Coffee Break: discussion

17:00-19h00 Strasbourg Visit

Free Evening

Thursday May 14th

8:30-9:30	<u>Keynote</u> State of the art in model order reduction <i>Wil Schilders (NXP Semiconductors & TU Eindhoven)</i>
9:30-11:00	Session 5: Linear Macromodeling Session chair: Wil Schilders, NXP Semiconductors & TU Eindhoven (NL)
9:30-9:50	Parameterized macromodels of multiconductor transmission lines <i>G. Antonini, F. Ferranti, T. Dhaene, L. Knockaert</i>
9:50-10:10	Black-box identification of delay-based macromodels from measured terminal responses <i>Piero Triverio, Stefano Grivet-Talocia, Alessandro Chinea</i>
10:10-10:30	Modeling Multi-Port Systems from Frequency Response Data via Tangential Interpolation <i>Sanda Lefteriu and Athanasios C. Antoulas</i>
10h30-10h50	Passivity Verification and Enforcement of Delayed Rational Function Macromodels from Networks Characterized by Tabulated Data <i>Andrew Charest, Michel Nakhla, Ram Achar, and Changzhong Chen</i>
11:00-11:30	Coffee Break
11:30-12:30	Session 6: On-Chip Interconnects Session chair: Hartmut Grabinski, Univ. Hannover, Institut für Theoretische Elektrotechnik, Hannover (D)
11:30-11:50	Polarization Mode Basis Functions for Modeling Insulator-Coated Through-Silicon Via (TSV) Interconnections <i>Ki Jin Han, Madhavan Swaminathan</i>
11:50-12:10	Equivalent Victim Model of the Coupled Interconnects for Simulating Crosstalk Induced Glitches and Delays <i>Shehzad Hasan, Ajoy K. Palit, Walter Anheier</i>
12:10-12:30	On the Quantification and Improvement of the Models for Surface Roughness <i>Brian Curran</i>
12:30-14:00	Lunch
14:00-15:20	Session 7: Signal and Power Integrity Session chair: Michel S. Nakhla, Carleton University, Department of Electronics, Ottawa (CAN)
14:00-14:20	Differential to Common Mode Conversion Due to Asymmetric Ground Via Configurations <i>Renato Rimolo-Donadio, Xiaomin Duan, Heinz-Dietrich Brüns, Christian Schuster</i>
14:20-14:40	Supply Voltage Drop Study Considering On-Chip Self Inductance of a 32-bit Processor's Power Grid <i>Daniel A. Andersson, Björn Nilsson, Johnny Pihl, Lars "J" Svensson, and Per Larsson-Edefors</i>
14:40-15:00	Extraction of Broadband Error Boxes for Microprobes and Recessed Probe Launches for Measurement of Printed Circuit Board Structures <i>Miroslav Kotzev, Renato Rimolo-Donadio, Christian Schuster</i>
15:00-15:20	Identification of Interconnect Failure Mechanisms Using RF Impedance Analysis <i>Daeil Kwon, Michael H. Azarian, and Michael Pecht</i>
15:20-17:00	Coffee Break & Poster Session
17:30	Social Event & Best Paper Award

Friday May 15th

9:00-10:20	Session 8: Linear Macromodeling Session chair: Madhavan Swaminathan, Georgia Institute of Technology, Atlanta (USA)
9:00-9:20	On the Construction of Uniformly Stable Multivariate Interconnect Macromodels <i>Piero Triverio, Stefano Grivet-Talocia, Michel Nakhla</i>
9:20-9:40	Fast Passivity Enforcement Technique for Common-Pole S-Parameter Multiport Systems <i>Dirk Deschrijver, Tom Dhaene</i>
9:40-10:00	Vector Fitting vs Levenberg-Marquardt : Some Experiments <i>L. Knockaert, F. Ferranti, T. Dhaene</i>
10:00-10:20	Identifying Bands of Passivity Violations For Scattering-Based Macromodels by a Half-Size Test Matrix <i>Bjorn Gustavsen</i>
10:20-10:50	Coffee Break
10:50-11:30	Session 9: Interconnect Modeling Session chair: Tom Dhaene, Ghent University (B)
10:50-11:10	Conductor Modeling with the Surface Admittance Operator of Triangles <i>Thomas Demeester, Daniël De Zutter</i>
11:10-11:30	Acceleration of Transverse Waveform Relaxation Using Waveform Compression <i>T. Maestri, I.M. Elfadel, A. Ruehli</i>
11:30	Closing

Poster Session

Thursday May 14th, 15:20-17:00

Session chair: Yves Quéré, Brest University, Lab-STICC (F)

Modeling the Interconnection of a Pseudo-Differential Link Using a Wide Return Conductor

Frederic Broyde, Evelyne Clavelier

Sensitivity of output response to geometrical dimensions in VLSI interconnects

Agnieszka Ligocka-Wardzińska, Wojciech Bandurski

Low-Impedance and High-Q Transmission Line for mmw VCO

You Nomiyama, Win Chaivipas, Kenichi Okada, and Akira Matsuzawa

BER Simulation for High-Speed Serial Links with Crosstalk, Noise, ISI and Jitter using Quasi-Analytical Method

Dingqing Lu, Chunxing Huang, Xiaoqing Dong and Daoxue Hu

Integral Power Net Integrity Analysis of a packaged u-Controller System including the u-Controller on-Chip Power Net Distribution

Ekkehard Miersch, Mehmet Goekcen, Thomas Steinecke

Effect of Underlayer Dummy Fills on On-Chip Transmission Line

Akira Tsuchiya and Hidetoshi Onodera

Towards Supply-Grid-Based Derating of Timing Margins

Svensson, Pihl, Andersson, Nilsson, Larsson-Edefors

Analysis of EMI Dependence on Signal Duty and Supplied Voltage

Pilsoo Lee, Jae-Kyung Wee, Inchaee Song, and Boo-Gyoun Kim

Measurement and simulation correlation of backplane serdes channel

Perry Qu