12th workshop on Signal Propagation on Interconnects
Avignon, May 12–15, 2008

Evolution and challenges of interconnect technologies and performance

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Outline

Introduction
- The place of interconnects among integrated circuits

Evolution of technologies with Moore’s law
- Impact of interconnects down sizing on performance
- Technological solutions under development

Optimization of BEOL stack propagation performance
- Definition of simulation condition based on real circuit analysis
- Extraction of process recommendations for the 32 nm node
- Investigation of variability impact on performance

Emerging interconnects
- 3D integration as an enabling solution

Summary
Different scales inside a chip

- 2x2 cm²
- 10x10 mm²
- 4x4 μm²
- 500x500 nm²

Introduction | Evolution of interconnects | Process optimization | 3D integration | Summary
Hierarchy of interconnects

Interconnect sizing
- Metal1 / local (ultra-dense)
  - Intra-cell routing
- Intermediate (very dense)
  - Inter-cell routing
- Global (relaxed dimensions)
  - Inter-block/core routing

Signal distribution
- Digital signals
- Clock distribution
- Power and ground
- Analog & RF
- Etc...

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Main interconnect parameters

Materials to meet R.C product expectations

⇒ Integration of Cu metallization to reduce resistivity
⇒ Introduction of porous insulators with Ultra Low K-values
Interconnect integration steps

Dual Damascene Trench First Hard Mask architecture

- Porous ULK
- Dielectric capping
- Metal barrier
- Cu
- Metal HM
- Dielectric HM
- PR
Technology scaling down with Moore’s law

<table>
<thead>
<tr>
<th></th>
<th>CMOS120</th>
<th>CMOS090</th>
<th>CMOS065</th>
<th>CMOS045</th>
<th>CMOS032</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>W (nm)</strong></td>
<td>200</td>
<td>140</td>
<td>100</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td><strong>S (nm)</strong></td>
<td>210</td>
<td>140</td>
<td>100</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td><strong>T (nm)</strong></td>
<td>350</td>
<td>330</td>
<td>220</td>
<td>140</td>
<td>100</td>
</tr>
<tr>
<td><strong>H (nm)</strong></td>
<td>400</td>
<td>290</td>
<td>160</td>
<td>120</td>
<td>80</td>
</tr>
</tbody>
</table>
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Summary
Interconnect performance

**Double integration density at each node**
- All interconnect dimensions scale down by a $\approx 0.71$ factor

**Ensure signal transmission speed and integrity**
- Wiring resistance and capacitance $\Rightarrow$ delay times
- Coupling capacitances $\Rightarrow$ crosstalk & delay uncertainty

**Limit power consumption across the chip**
- Reduce capacitance for dynamic power budget
- High current densities in resistive lines lead to voltage drops

**Guarantee the most reliable integrated circuits**
- Electromigration and stress-migration $\Rightarrow$ circuit lifetime

**Reduce variability to improve circuit robustness**
Resistance: size does matter

Progressive scaling down of conductive sections

- Resistivity increase due to scattering effects

**Surface Scattering**

**Grain Boundary Scattering**

Source: ITRS 2005

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Evolution of performance

- Capacitance decreases with k-value
- But R.C increases sharply due to R
Capacitance or resistance driven delay

Notion of critical length

- Interconnect resistance increasingly affects delay times
- Wide drivers are no longer sufficient to load capacitances

⇒ Critical length is of a few tens of µm for the 32 nm node
Evolution of crosstalk

Impact of coupling capacitances

- Capacitive crosstalk roughly proportional to $k_c = \frac{C_{IMD}}{C_{ILD}}$
- Mainly fixed by the aspect ratio of lines and vias
- **Crosstalk level increases** at each new generation

- Induces delay uncertainty
- **Delay increased by crosstalk** up to 3x classical delay
Dynamic power

Increase of dynamic power in the interconnect stack

- Interconnects contribute significantly to dynamic power
- \( P = N \cdot A \cdot F \cdot C \cdot V^2 \) (functionality \( N \), activity \( A \), frequency \( F \))
- Power per GHz per cm\(^2\) of metal layer

\[
\begin{array}{cccccc}
90 & 65 & 45 & 32 & 22 & 16 \\
\hline
0.75 & 1 & 1.25 & 1.5 & 1.75 & 2 \quad \text{(upper value)} \\
0.75 & 1 & 1.25 & 1.5 & 1.75 & 2 \quad \text{(lower value)}
\end{array}
\]

Source: ITRS (2007)

\( \Rightarrow \) Interconnect capacitances drive dynamic power
Electromigration in Cu interconnects

Mass transport under electron wind driving force

- Increase of current densities at each generation
- Vacancies

Multiple diffusion pathways

- Interface with dielectric capping
- Grain boundaries
- Interface with metal barrier
Performance through technological innovations

Compensation of resistance increase

- Highly conformal and very thin metal barriers
- Sidewalls roughness and Cu grain size

Chip lifetime improvement

- Introduction of self-aligned barriers (ex: CoWP, CuSiN, ...)
- Improvement of line interfaces with copper alloys (ex: CuAl)

Decrease of parasitic capacitances

- Increase of insulator porosity to reduce k-value
- ULK dielectric restoration to preserve its integrity
- Thin low-k dielectric barriers and capping layers
- Integration of air gaps to reach extremely low k-values

⇒ Potential solutions under development within labs & IDM
Resistance: thin metal barriers

Reduction of metal barrier thickness

- Metal barrier is no longer negligible
- Thin metal barriers enlarge Cu volume
  - Balance electron scattering effect
  - Increase Cu conductive section

\[ W_{Cu} = W_{line} - 2W_{TaN} \]

- ALD barrier (2 nm)
- PVD barrier (16 nm)
Electromigration: copper alloys

Copper doping to seal interfaces

- Improvement of copper to barrier adhesion
- Al atoms diffuse to grain boundaries during anneal
  ➔ Improvement of electromigration lifetime

ALD TaN/Cu after 400°C anneal
ALD TaN/CuAl after 400°C anneal

Other Cu alloys under investigation (CuMn)
Electromigration: self-aligned barriers

Selective electroless deposition of CoWB/P

- Improved electromigration lifetime
- Useful for air gap integration

Standard SiCN  Self-aligned barrier

Alternative approach with CuSiN line surface modification
## Capacitance: porous dielectrics

### Roadmap for k-value reduction

- Progressive reduction of inter-metal dielectric k-value

<table>
<thead>
<tr>
<th>Technology node (nm)</th>
<th>130</th>
<th>90</th>
<th>65</th>
<th>45</th>
<th>32</th>
<th>22</th>
</tr>
</thead>
<tbody>
<tr>
<td>K-value</td>
<td>3.9</td>
<td>3.1</td>
<td>2.9</td>
<td>2.5</td>
<td>2.3</td>
<td>≤ 2.1</td>
</tr>
<tr>
<td>Material</td>
<td>FSG</td>
<td>SiOC</td>
<td>SiOC</td>
<td>Porous SiOC</td>
<td>Porous SiOC</td>
<td>Air gap</td>
</tr>
<tr>
<td>Porosity</td>
<td>25%</td>
<td></td>
<td></td>
<td>30%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

⇒ Introduction of porous materials for sub 65 nm nodes
Capacitance: porous dielectrics (cont’d)

**Introduction of porosity to reduce k-value**

- Two compound mixture deposition: matrix material + porogen
- Curing for porogen removal and porosity generation
- Additional UV cure treatment for mechanical robustness

![Graph showing K value vs. porogen ratio in gas feed (au)]

**Porogen ratio in gas feed (au)**

<table>
<thead>
<tr>
<th>Porogen ratio in gas feed (au)</th>
<th>K value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>3.0</td>
</tr>
<tr>
<td>1.0</td>
<td>2.8</td>
</tr>
<tr>
<td>1.2</td>
<td>2.6</td>
</tr>
<tr>
<td>1.4</td>
<td>2.4</td>
</tr>
<tr>
<td>1.6</td>
<td>2.2</td>
</tr>
</tbody>
</table>
Capacitance: from low-k to no k

Introduction of air gap architectures

- Creation of air gaps with non-conformal deposition
- Removal of sacrificial materials after multi-level interconnects

Non-conformal deposition

Sacrificial material

⇒ k-values ≥ 1.7 have been demonstrated with air gap
Capacitance: low-k dielectric capping

Growing influence of dielectric barrier

- Strong impact on effective k-value
- Capacitance degradation

⇒ Development of dielectric capping with k-values ≤ 4
Challenges of technological solutions

Thin metal barriers
- Copper diffusion
- Adhesion on dielectric

Copper alloys and self-aligned barriers
- Resistance increase due to inter-diffusion
- Compatibility with standard integration flows

Porous insulators and low-k dielectric capping
- Diffusion of metal barrier and copper
- Tuning of porosity to decrease the k-value
- Mechanical stability & compatibility with packaging
- Degradation during integration processes (CMP, etch, ...)

⇒ Need for recommendations to develop the right solutions
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Summary
Objective: optimization of CMOS032 BEOL stack

Performance driven process recommendations

Objective: improve performance by 17% vs 45 nm node

Process parameters of interest

- Metal and via heights
- **ULK dielectric** k-value and integrity
- **Capping layers** k-value and thickness
- **Metal barrier** resistivity, thickness and impact on line resistivity
Definition of propagation performance criteria

Time domain analysis of interconnect properties

- Extraction of delay, crosstalk and delay increased by crosstalk
- Results are function of **driver size** and **interconnect length**
Prediction of interconnect performance

Wire length impact on circuit performance varies

- Minimized critical path for logic area (a few tens of µm)
- Long bit & word lines in memories (several hundreds of µm)

Ring oscillators timing responses (MASTAR)

⇒ Delay time = f(driver and wire)
⇒ Right driver/wire conditions?

⇒ Performance strongly depends on considered application
Analysis of a real circuit

Wiring network

- Real USB controller with many functional blocks
- Total interconnect length distribution of inter-cell layout

⇒ Follows the Rent’s rule

⇒ Critical interconnects are dispatched among $M_x$ levels
Analysis of a real circuit (cont’d)

**Driver characteristics**

- Extraction of **minimum driver size** adequate to load wires
- Driver size distribution versus interconnect length

![Graph showing interconnect length vs. driver size](image)

- $l_{\text{int}} = 10 \, \mu m$, drivers 2x
- $l_{\text{int}} = 100 \, \mu m$, drivers 4x
- $l_{\text{int}} = 200 \, \mu m$, drivers 7x
- $l_{\text{int}} = 500 \, \mu m$, drivers 18x
- $l_{\text{int}} = 1 \, mm$, drivers 62x

⇒ **Definition of five test cases covering most applications**
Identification of critical elements

Modeling of wiring

- Interconnect RLC model
- Access resistance to input driver
- Vertical contact and via connections

⇒ Electrical modeling with technological parameters
Identification of critical elements

Comparative study of parameters influence

- Repartitions of parameter impacts as a function of line length

\[ l_{\text{int}} = 10 \, \mu m \]
Drivers 2x

\[ l_{\text{int}} = 100 \, \mu m \]
Drivers 4x

\[ l_{\text{int}} = 500 \, \mu m \]
Drivers 18x

\[ l_{\text{int}} = 1 \, mm \]
Drivers 62x

⇒ Slight influence of \( R_{\text{contact}} \) compared to silicide interfaces
⇒ Drivers mainly affect transmission speed for short wires
Identification of critical elements

Influence of interconnect parameters

- Applications driven by short wires are limited by $C_{BEOL}$
- R.C product is representative of long lines performance
Protocol for performance prediction

Simulation methodology

- A design of experiment drives the definition of test cases
- Electromagnetic simulations to extract RLCG(ω) matrixes
- Time domain calculations leading to voltage responses
- Statistical analysis tool for optimization and variability

Definition of BEOL technology stack

Electromagnetic simulations

Calculation of transmitted signals

Introduction | Evolution of interconnects | Process optimization | 3D integration | Summary
Investigated BEOL stack

Extraction of electrical parameters

- BEOL stack from silicon to encapsulation (contact, vias, ...)
- Three coupled interconnects between two ground planes
- Integrated material properties (k-values and resistivities)

Introduction
| Evolution of interconnects | Process optimization | 3D integration | Summary |

Metal X

Metal X+1

Metal barrier

ILD low-k insulator

IMD low-k insulator

Dielectric HM

Dielectric barrier

Copper
Material evaluation: metal barrier

Resistance decrease with metal barrier

- Reduction of barrier thickness
- Increases effective copper conductive section
- Relax electron scattering effects affecting Cu resistivity

Transmission speed improvement for long interconnects

⇒ Process optimization | 3D integration | Summary
Material evaluation: porous insulator

Capacitance reduction with ULK dielectric
- Reduction of insulator k-value through porosity increase
- Impact of the remaining dielectric hard mask
  - Higher k-value which increases overall effective k-value

⇒ 5% speed improvement with ULK but capping is critical
Impact of geometry and materials

Modeling of relative influences of all parameters

Comparison of effects for an interconnect length of 100 μm

For delay time
- ULK dielectric 35%
- Capping layer 22%
- Stack heights 21%
- Metal barrier 13%

⇒ Short wires optimization has to focus on all insulators

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14th of May 2008, Avignon
Alexis FARCY 37
Extraction of material requirements for delay

Comparison of metallization and dielectric effects

- Dielectric influences decrease with interconnect length
- Metal barrier thickness is dominant for $L \geq 140 \, \mu m$

Recommendations from optimization

- ULK insulator $k \leq 2.35$
- Dielectric capping $k \leq 4$
- Metal barrier thickness $\leq 5 \, \text{nm}$
Optimization of geometrical parameters

Evolution of dimensional influences with length

- Opposite trends for via height and metal thickness vs length
- Balance between line resistance and capacitance

Recommendations from optimization

- Line width density → 50 nm
- Line aspect ratio A/R = 2
- Via aspect ratio A/R = 3.6
**Impact of process variability on R-C**

**The variability challenge**
- Intra-chip, chip-to-chip and wafer-to-wafer variability
- Variability is design (OPC, density...) and process dependent

**Monte-Carlo simulations**

**Dimensions ($\sigma = 10\%$)**
- Line width
- Metal thickness
- Via height

**Materials ($\sigma = 10\%$)**
- Dielectric $k$-values
- Dielectric thicknesses
- Metal barrier thickness

⇒ Strong impact of process variability on R.C product

$\sigma_C = 11\%$
$\sigma_R = 22\%$
**Effect of variability on performance**

**Propagation performance**

- Impact of 10 % process variability for 100 µm long lines
- Delay, crosstalk and delay increased by crosstalk

![Graphs showing delay, crosstalk, and delay uncertainty with varying standard deviation](image)

- Delay is less impacted by variability than R.C product
- Short wires are also sensitive to device variability

⇒ Impact of short line process variability is limited to 5 %
Variability as a function of wire length

Evolution of performance sensibility to variability

- Delay, crosstalk and delay uncertainty variations with length

![Graph showing variability impact on delay increases with line length](image)

⇒ R variability impact on delay increases with line length
Geometrical versus material variability

Contributions to delay variability

- Delay variations
  - with dimensions uncertainty
  - with variations of material properties

Performance variability is mainly related to dimensional variations (lithography, etching and polishing)
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Summary
Emerging interconnects

Interconnects strongly limit circuit performance

Alternative interconnect systems

- Use different signaling methods
  - Signal design
  - Signal coding techniques
  - Chip-package co-design with packaged interconnects

- Introduce new enabling technologies
  - 3D integration
  - Optics (waveguides, emitters, detectors, free space, trans-impedance amps, modulators)
  - Wireless (transmitters, receivers, free space, waveguides)
  - Nanowires / nanotubes / graphene

⇒ 3D integration seems to be a very promising solution
Introduction to 3D integration

**Principle**
- Stacking of multiple chips with vertical interconnections

**Technological challenges**
- Completion of vertical interconnects (TSV) to ensure signal transmission
- Bonding with alignment of functional dies
- Substrate thinning and handling of resulting stack

⇒ Development of dedicated processes needed for 3D
Interests for 3D integration

- **Performances driven**
  - "Mid term" driver: > 2010
  - Heterogeneous integration
    - Co-integration of RF + logic + memory + sensors in a reduced space

- **Cost driven**
  - "Long term" driver: > 2012

- **Form factor driven**
  - "Short term" driver: > 2008
  - Achieving the highest capacity / volume ratio

- **3D vs. “More Moore”**
  - Can 3D be cheaper than going to the next lithography node?

Source: J.C. Eloy, EMC 3D workshop (2007)
Interest for system integration

Stacking of specialized heterogeneous substrates

- Evolution of 2D SoC toward 3D system integration
- Dedicated technologies (logic, memories, analog, passives, ...)

Introduction | Evolution of interconnects | Process optimization | 3D integration | Summary
Interest for circuit performance

Reduction of global interconnect length

- Long interconnects are replaced by vertical interconnects
- Global delay and power consumption are reduced

Interest for integration cost

Reduction of manufacturing costs

- Highly integrated logic circuit (300 mm technologies)
- I/Os and analog functionalities with non critical generation
  ➔ Strong manufacturing cost reduction prevision

Logic circuit (std cells)

I/Os

Analog functions

Mature node

Advanced node

Area 2.A

Area A
Worldwide development of 3D technologies

Companies involved in 3D

- 3D start ups
  - ALL VIA
  - CUBIC WAFER
  - ziptronix
  - ZyCube

- Memories
  - ELPIDA
  - Qimonda
  - Tezzaron
  - Samsung
  - Micron

- IDM
  - Intel
  - Toshiba
  - Sharp
  - Hitachi

- Foundries
  - OKI
  - STATSchipPAC
  - TESSERA
  - NEX
  - Fujikura

- Packaging
  - Chartered Semiconductor Manufacturing
  - STMicroelectronics

⇒ 3D integration is becoming a "must have" technology
Application roadmap for 3D integration

Low density 3D via Chip-level bonding

2007 2009 2012 >2014

High density 3D via wafer-level bonding

Vertical device on CMOS (NTC, NW, NEMS)

Vertical 3D via pitch (µm)

Vertical Interconnect Density (cm⁻²)

1E9 1E8 1E7 1E6 1E5 1E4 1E3 1E2 10 0.1

CMOS Image sensor (Sensor + DSP + RAM)

Via size=50µm

Flip chip solder bump min pitch

Via size=5-30µm

3D Stacked memory (NAND, DRAM, …)

Source: P. Leduc, EMC 3D workshop (2007)
Example of 3D integration approach

High-density TSV from IMEC

- Realization of **Via first TSV** between FEOL and BEOL
- Bonding on temporary carrier and Si thinning
- Die to wafer stacking with dielectric + Cu to Cu bonding

Source: G. Druais, MAM (2008)
Example of 3D integration approach (cont’d)

High density TSV from CEA LETI

- **Via last** approach
- Face-to-face
- SiO₂ Direct bonding
- Alignment < 1.5 μm
- Top Si thinning (< 10 μm)

Source: M. Rousseau, IMAPS (2008)
3D integration challenges

From a technology perspective
- Process steps for medium and high density TSV realization
- Bonding techniques for die stacking with good alignment
- Silicon thinning and handling technologies

Concerning performance
- TSV propagation characteristics and frequency behavior
- Impact of lossy silicon substrate on chip performance
- Electrical and mechanical influence of TSV on devices
- Thermal dissipation and reliability of stacked circuits

From a design point of view
- System partitioning using 3D design tools and methodology

⇒ 3D integration is a brand new field requiring design, characterization, modeling & technological developments
Summary

Interconnect propagation performance

- Advanced technology nodes are in the **nanometric scale**
  - Line section will be 50 nm x 100 nm for CMOS032
  - Section shrink and **resistivity increase**
  - Interconnect is the **most limiting factor** affecting IC speed

- Need for performance driven process recommendation
  - Methodology based on predictive simulation within DOE
  - Optimization of the technological stack for CMOS032

- But technology is not sufficient
  - **Design optimization** required (resistance, variability, ...)

Alternative interconnect systems

- Industry will move to **3D integrated systems**
  - Very promising solution for density, performance & cost
Forecast

Modeling tools to address technological innovations

More Moore
- Increasingly significant layers (TaN, SiCN, ...)
- Complex geometries & architectures (CoWP, Air Gap, ...)
- Form factors (from a few nm to mm long lines)
- Introduction of lossy porous dielectrics (G ≠ 0)

More than Moore
- New interconnecting systems
Acknowledgement

Thank you for your attention